What is claimed is:

1. A method comprising:

scheduling processing of a packet received by a packet processor with a hardware scheduler in a stack processor included in the packet processor.

2. The method of claim 1 wherein the scheduling includes receiving an interrupt signal from a packet engine included in the packet processor.

3. The method of claim 1 wherein the scheduling includes identifying an interrupt handling routine.

4. The method of claim 2 wherein a control processor in the packet processor manages the packet engine.

5. The method of claim 1 wherein the scheduler uses a weighted round robin scheduling scheme.

6. The method of claim 1 wherein the stack processor receives the packet for a scratch ring included in the packet processor.

7. The method of claim 4 wherein the stack processor passes a message through a communication queue to the control processor.

8. A computer program product, tangibly embodied in an information carrier, the computer program product being operable to cause a machine to:

schedule processing of a packet received by a packet processor with a hardware scheduler in a stack processor included in the packet processor.

9. The computer program product of claim 8 wherein instructions to schedule include instructions to receive an interrupt signal from a packet engine included in the packet processor.

10. The computer program product of claim 8 wherein the instructions to schedule include instructions to identify an interrupt handling routine.

11. The computer program product of claim 9 wherein a control processor in the packet processor manages the packet engine.

12. The computer program product of claim 8 wherein instructions to schedule use a weighted round robin scheduling scheme.

13. The computer program product of claim 8 wherein the stack processor receives the packet from a scratch ring included in the packet processor.

14. The computer program product of claim 11 wherein the stack processor passes a message through a communication queue to the control processor.

15. A scheduler comprises:

a process to schedule processing of a packet received by a packet processor with a hardware scheduler in a stack processor included in the packet processor.

16. The scheduler of claim 15 wherein the scheduling includes receiving an interrupt signal from a packet engine included in the packet processor.

17. The scheduler of claim 15 wherein the scheduling includes identifying an interrupt handling routine.

18. A system comprising:

a packet processor capable of,

scheduling processing of a packet received by the packet processor with a hardware scheduler in a stack processor included in the packet processor.

19. The system of claim 18 wherein scheduling includes receiving an interrupt signal from a packet engine included in the packet processor.

20. The system of claim 18 wherein scheduling includes identifying an interrupt handling routine.

21. A packet forwarding device comprising:

an input port for receiving packets;

an output for delivering the received packets; and

a packet processor capable of,

scheduling processing of a packet received by the packet processor with a hardware scheduler in a stack processor included in the packet processor.

22. The packet forwarding device of claim 21 wherein scheduling includes receiving an interrupt signal from a multithreaded packet engine included in the packet processor.

23. The packet forwarding device of claim 21 wherein scheduling includes identifying an interrupt handling routine.

24. A packet processor comprising:

a packet engine for receiving a packet;

a control processor for managing the packet engine; and

a stack processor for scheduling processing of the received packet with a hardware scheduler.

25. The packet processor of claim 24 wherein the stack processor receives an interrupt signal from the packet engine.

26. The packet processor of claim 24 wherein the hardware scheduler identifies an interrupt handling routine.